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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,866	03/30/2004	Christopher J. Diorio	IMPJ-0027B	5628

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EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/814,866	DIORIO ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,14,16,18-22,27,28,30,33,39-44,49,50,54,55,74-113* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14,16,18-22,27,28,30,33,39-44,49,50,54,55,74-84,87-99 and 102-113* is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☒ Claim(s) *85,86,100 and 101* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004 and 30 May 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's amendment flied 10/19/07 has been received and entered in the case. Claims 1-7 are rejected and Applicant's arguments are addressed below.

Claim Objections

Claims 85, 86, 100 and 101 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claims 85, 86, 100, 101 recite "wherein said" first/second "nonvolatile memory element comprises a first floating-gate transistor having a" first/second "floating gate, an amount of the charge on the" first/second "floating gate determining said" first/second "memory value". These above limitations are already recited in the independent claims 84 and 99 from which 85, 86, 100 and 101 depend (for instance, see lines 8-12 of claim 84). It is suggested that the above claims be cancelled.

Specification

The amendment filed 10/19/07 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

There is no support in the original disclosure for an electronic fuse having a logic gate to establish a first configuration of a circuit controlled by the fuse "in which the circuit operates in a first operative state" and establishes a second configuration of the circuit "in which the circuit operates in a second operative state different from the first operative state" as recited in claim 1.

Applicant is required to cancel the new matter in the reply to this Office Action.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the circuit that "operates in a first operative state" and "operates in a second operative state different from the first operative state" responsive to a logic gate of the electronic fuse must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering

of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There is no support in the original disclosure for the limitations of an electronic fuse having a logic gate to establish a first configuration of a circuit controlled by the fuse "in which the circuit operates in a first operative state" and establishes a second configuration of the circuit "in which the circuit operates in a second operative state different from the first operative state" as recited in claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, and 4-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Pascucci (USPN 5,854,762)

With respect to claim 1, Pascucci discloses in Fig. 2, a device comprising:

a logic gate (latched inverters of 6) having an output node connected to the circuit (output of 6 is coupled to a circuit, i.e., 8, which is controlled by 6 via node 03, i.e., UGVdis supplied to M15 and M19 of Fig. 2);

at least one nonvolatile memory element (M1 of 3), said at least one nonvolatile memory element configured to be programmed to a memory value capable of causing the output of said logic gate to settle to one of a first and second predetermined states as a power-up or a reset signal is applied to the fuse (when the POR signal is applied to the fuse at node 16 as a low voltage signal, M5 will turn on to allow the value stored in M1 to be supplied to 6, thus controlling the logic value, i.e., high or low, of the output of 6), the first predetermined state of the output of the logic gate establishing a first configuration (the first predetermined state corresponds to when the voltage level DIS at

the gate of M1 is too low, i.e., below the threshold of M1. At this point 6 is controlled to provide a low signal as UGVdis. Thus, "the circuit" 8 is configured to be turned on, i.e. M15 is activated, so that the voltage at X3 follows Vdd) in which the circuit operates in a first operative state (clearly 8 operates to "follow Vdd" in the first operative state by controlling M15 to be conductive), the second predetermined state of the output of the logic gate establishing a second configuration of the circuit in which the circuit operates in a second operative state different from the first operative state (the second state is when DIS is at or above the threshold of M1, thus turning on M1 to pull DW of 6 low to supply a high UGVdis. Thus, UGVdis turns on, i.e., activates, M19 to pull X3 low, therefore operating the circuit 8 in a second configuration, i.e., operating M19 so that 8 outputs a low signal. Furthermore, it can be seen that the limitations of the operating the "the circuit" in first and second operative states is merely intended used of the "electronic fuse").

With respect to claim 2, Pascucci discloses, that M1 is a floating a gate transistor wherein the amount of charge on said gate determines the memory value.

With respect to claims 4, Pascucci discloses, M1 is fabricated by a MOS process.

With respect to claims 5, Pascucci discloses, M1 is a floating gate transistor fabricated by a MOS process.

With respect to claims 6, Pascucci discloses, that M1 uses dielectric change to store information, since the control gate of M1 is capacitively coupled to the floating gate through a dielectric layer (see Col. 1 lines 34-36).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 7are rejected under 35 U.S.C. 103(a) as being unpatentable over Pascucci et al. (USPN 5,854,762) in view of Dugger et al. (USPAPN 2003/0183871).

With respect to claim 3, Pascucci et al. fails to disclose the floating gate nonvolatile memory element M1 having a first and second capacitor coupled to its floating gate. However, it is notoriously well-known in the art that floating gate transistors are composed of a first capacitor having a first plate in common with a floating gate of a floating gate transistor and a second "tunneling" capacitor having a plate in common with the floating. This is further evidenced, in Fig. 5 of Dugger et al., which discloses a nonvolatile memory transistor which has "a first capacitor having a first plate (572) in common with the floating gate (566) of said floating-gate transistor (520)" and "a second capacitor having a first plate (571) in common with the floating gate (566) of said floating gate transistor (520) Dugger et al.'s capacitor allows for increased flexibility in programming the nonvolatile memory.

It would have been obvious for one of ordinary skill in the art at the time of the invention to use the specific floating gate transistor 520 of Fig. 5 of Dugger et al. in place of the generic floating gate transistor of M1 of Pascucci et al. for the purpose of having a floating gate transistor with an increased flexibility in programming the transistor.

With respect to claim 7, the above combination discloses, changing the amount of charge on the floating gate using Fowler-Nordheim tunneling and hot-electron injection (see paragraph 0045 of Dugger et al.).

Response to Arguments

Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Furthermore, as can be seen in the above modified rejection Pascucci does, in fact, disclose a circuit controlled in a first and second operative state. Moreover, the above limitations with respect to the first and second operative states of the circuit controlled by the electronic fuse is merely intended use of the claimed "electronic fuse circuit".

Allowable Subject Matter

Claims 14, 16, 18-22, 27, 28, 30, 33, 39-44, 49, 50, 54, 55, 74-84, 87-99 and 102-113 are allowed. .

The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 14, 16, 18-22, 27, 28 and 30, there is no cited art that discloses, the specific master latch having a cross-coupled latch with sized gate-width-to length ratios of the transistors of the cross-coupled inverters in the specific "electronic fuse" as recited in claim 14.

With respect to claims 33, 39-44, 49, 50, 54 and 55, there is no cited art that discloses, the first output of a master latch being capacitively coupled to a first source of a fixed voltage and a second output being capacitively coupled to a second source of a fixed voltage that is the same as the first in the specific "electronic fuse" as recited in claim 33.

With respect to claims 74-83, there is no cited art that discloses, the specific master latch having a cross-coupled latch with a doping level of one of the transistors of the cross-coupled inverters being different than a doping level of another transistor of the cross-coupled inverters in the specific "electronic fuse" as recited in claim 74.

With respect to claim 84 and 87-98, there is no cited art that discloses, the specific master latch having a cross-coupled latch with sized gate-width-to length ratios of the transistors of the cross-coupled inverters in the specific "electronic fuse" as recited in claim 84.

With respect to claim 99, there is no cited art that discloses, the specific master latch having a cross-coupled latch with a doping level of one of the transistors of the

cross-coupled inverters being different than a doping level of another transistor of the cross-coupled inverters in the specific "electronic fuse" as recited in claim 99.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm. If attempts to reach the examiner by telephone are unsuccessful,

the examiner's supervisor, Drew Richards, can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH
December 13, 2007

N. DREW RICHARDS
SUPERVISORY PATENT EXAMINER